IN THE CLAIMS:

1. (currently amended) For use with a circuit having first and second complementary drivers exhibiting different current gain characteristics, said first driver having a plurality of vertical PNP transistors, a balancing circuit, comprising:

a sensing subcircuit configured to provide a correction signal indicating a first current gain characteristic of said first driver; and

a compensation subcircuit configured to generate a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal.

2. (canceled)

3. (currently amended) For use with a circuit having first and second complementary drivers exhibiting different current gain characteristics, ~~The balancing circuit as recited in Claim 1 wherein~~ said second driver ~~comprises~~ having a plurality of vertical NPN transistors, a balancing circuit, comprising:

a sensing subcircuit configured to provide a correction signal indicating a first current gain characteristic of said first driver; and

a compensation subcircuit configured to generate a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal.

4. (original) The balancing circuit as recited in Claim 1 wherein said sensing subcircuit comprises at least one diode-connected transistor configured to substantially replicate said current gain characteristic of said first driver.

5. (original) The balancing circuit as recited in Claim 1 wherein said compensation subcircuit comprises a current repeater.

6. (currently amended) For use with a circuit having first and second complementary drivers exhibiting different current gain characteristics, a balancing circuit, comprising:

a sensing subcircuit configured to provide a correction signal indicating a first current gain characteristic of said first driver; and

a compensation subcircuit ~~The balancing circuit as recited in Claim 1 wherein said compensation subcircuit comprises~~ having emitter coupled logic configured to generate a ~~provide said~~ current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal.

7. (currently amended) For use with a circuit having first and second complementary drivers exhibiting different current gain characteristics, a balancing circuit, comprising:

a sensing subcircuit configured to provide a correction signal indicating a first current gain characteristic of said first driver; and

a compensation subcircuit configured to generate a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal, ~~The balancing circuit as recited in Claim 1~~ wherein said first and second current gain characteristics comprise a ratio of collector-to-base current of devices associated with said first and second drivers.

8. (currently amended) For use with a circuit having first and second complementary drivers exhibiting different current gain characteristics, said first driver having a plurality of vertical PNP transistors, a method of operating a balancing circuit, comprising:

providing a correction signal indicating a first current gain characteristic of said first driver; and

generating a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal.

9. (canceled)

10. (currently amended) For use with a circuit having first and second complementary drivers exhibiting different current gain characteristics, ~~The method as recited in Claim 8 wherein~~ said second driver having ~~comprises~~ a plurality of vertical NPN transistors, a method of operating a balancing circuit, comprising:

providing a correction signal indicating a first current gain characteristic of said first driver; and

generating a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal.

11. (original) The method as recited in Claim 8 wherein said providing is performed by a sensing subcircuit including at least one diode-connected transistor that substantially replicates said current gain characteristic of said first driver.

12. (original) The method as recited in Claim 8 wherein said generating is performed by a compensation subcircuit including a current repeater.

13. (currently amended) For use with a circuit having first and second complementary drivers exhibiting different current gain characteristics, a method of operating a balancing circuit, comprising:

providing a correction signal indicating a first current gain characteristic of said first driver; and

generating ~~The method as recited in Claim 8 wherein said generating is performed~~ by a compensation subcircuit including emitter coupled logic ~~a that provides said~~ current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal.

14. (currently amended) For use with a circuit having first and second complementary drivers exhibiting different current gain characteristics, a method of operating a balancing circuit, comprising:

providing a correction signal indicating a first current gain characteristic of said first driver; and

generating a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal, ~~The method as recited in Claim 8~~ wherein said first and second current gain characteristics comprise a ratio of collector-to-base current of devices associated with said first and second drivers.

15. (currently amended) A phase locked loop (PLL) circuit, comprising:

a voltage controlled oscillator, coupled to a filter circuit, that receives a signal associated with a charging signal and provides an output signal having an output frequency;

a comparator circuit that provides a comparison signal proportional to a phase difference between said output signal having said output frequency and an input reference signal having an input frequency; and

a charge pump that provides said charging signal via first and second complementary drivers exhibiting different current gain characteristics, said charge pump employing a balancing circuit, including:

a sensing subcircuit that provides a correction signal indicating a first current gain characteristic of said first driver, said first driver having a plurality of vertical PNP transistors; and

a compensation subcircuit that generates a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal.

16. (canceled)

17. (currently amended) A phase locked loop (PLL) circuit, comprising:

a voltage controlled oscillator, coupled to a filter circuit, that receives a signal associated with a charging signal and provides an output signal having an output frequency;

a comparator circuit that provides a comparison signal proportional to a phase difference between said output signal having said output frequency and an input reference signal having an input frequency; and

a charge pump that provides said charging signal via first and second complementary drivers exhibiting different current gain characteristics, said charge pump employing a balancing circuit, including:

a sensing subcircuit that provides a correction signal indicating a first current gain characteristic of said first driver; and

a compensation subcircuit that generates a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal, ~~The PLL circuit as recited in Claim 15 wherein~~ said second driver having ~~comprises~~ a plurality of vertical NPN transistors.

18. (original) The PLL circuit as recited in Claim 15 wherein said sensing subcircuit comprises at least one diode-connected transistor that substantially replicates said current gain characteristic of said first driver.

19. (original) The PLL circuit as recited in Claim 15 wherein said compensation subcircuit comprises a current repeater.

20. (currently amended) A phase locked loop (PLL) circuit, comprising:

a voltage controlled oscillator, coupled to a filter circuit, that receives a signal associated with a charging signal and provides an output signal having an output frequency;

a comparator circuit that provides a comparison signal proportional to a phase difference between said output signal having said output frequency and an input reference signal having an input frequency; and

a charge pump that provides said charging signal via first and second complementary drivers exhibiting different current gain characteristics, said charge pump employing a balancing circuit, including:

a sensing subcircuit that provides a correction signal indicating a first current gain characteristic of said first driver; and

a compensation subcircuit ~~The PLL circuit as recited in Claim 15 wherein said compensation subcircuit~~ having ~~comprises~~ emitter coupled logic that generates a ~~provides said~~ current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal.

21. (currently amended) A phase locked loop (PLL) circuit, comprising:

a voltage controlled oscillator, coupled to a filter circuit, that receives a signal associated with a charging signal and provides an output signal having an output frequency;

a comparator circuit that provides a comparison signal proportional to a phase difference between said output signal having said output frequency and an input reference signal having an input frequency; and

a charge pump that provides said charging signal via first and second complementary drivers exhibiting different current gain characteristics, said charge pump employing a balancing circuit, including:

a sensing subcircuit that provides a correction signal indicating a first current gain characteristic of said first driver; and

a compensation subcircuit that generates a current gain compensation signal to said first driver to substantially match a second current gain characteristic of said second driver based on said correction signal, ~~The PLL circuit as recited in Claim 15~~ wherein said first and second current gain characteristics comprise a ratio of collector-to-base current of devices associated with said first and second drivers.

22. (new) The balancing circuit as recited in Claim 3 wherein said sensing subcircuit comprises at least one diode-connected transistor configured to substantially replicate said current gain characteristic of said first driver.

23. (new) The balancing circuit as recited in Claim 3 wherein said compensation subcircuit comprises a current repeater.

24. (new) The method as recited in Claim 10 wherein said providing is performed by a sensing subcircuit including at least one diode-connected transistor that substantially replicates said current gain characteristic of said first driver.

25. (new) The method as recited in Claim 10 wherein said generating is performed by a compensation subcircuit including a current repeater.

26. (new) The PLL circuit as recited in Claim 17 wherein said sensing subcircuit comprises at least one diode-connected transistor that substantially replicates said current gain characteristic of said first driver.

27. (new) The PLL circuit as recited in Claim 17 wherein said compensation subcircuit comprises a current repeater.